HPC FEATURE OVERVIEW

Why Consider ARM-Based Servers For HPC?

ARM offers three specific, highly attractive advantages for HPC system designers:

- CPU Instruction Set Architecture (ISA) that can be optimized for specific workloads – resulting in substantial performance advantages
- Significantly lower energy consumption profile
- Substantially smaller footprint consumption design

Fujitsu's proprietary design added even more capability with the introduction of Scalable Vector Extensions (SVE) to the ARM ISA.

Further, Fujitsu leveraged a System-On-A-Chip (SOC) design using a 52 core ARM CPU with SVE, on-chip high bandwidth 32GB memory and an on-chip network for intra-node and inter-node communication.

The high-bandwidth on-chip memory is a key element in the compute node design as the high memory bandwidth significantly improves the computational capability while the high-speed interconnect network is used to meet the memory capacity needs for the MPI aggregation and collective operations.

As researchers are finding ways to augment traditional HPC applications, the need for high bandwidth memory and large-scale systems is growing at a rapid rate. This simplified ARM System-On-A-Chip design makes it easy to scale horizontally while maintaining a low energy consumption profile.

In summary, the major goal of the ARM Instruction Set Architecture (ISA) is to provide the flexibility to tailor to specific workloads/domains. It is found embedded in low-end devices, mobile phones, some server class machines and, most notably, in the world's fastest supercomputer, Fujitsu's Fugaku. This has become a game changer, as HPC and Supercomputer system designers now have access to a low cost, energy efficient platform that can be tailored to meet their specific workloads. In an environment where applications are getting more complex, the ability to scale without concerns about energy and space consumption is a big advantage over general-purpose systems that carry along excess resources not needed for the workload task but integral to the system design.

A64FX Technologies: Scalable Architecture

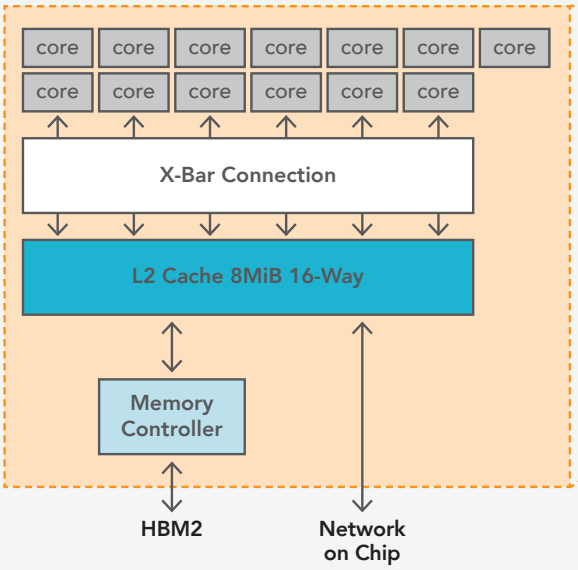
Core Memory Group (CMG)

- 12 compute cores for computing and an assistant core fior OS daemon, I/O, etc.
- Shared L2 cache
- Dedicated memory controller

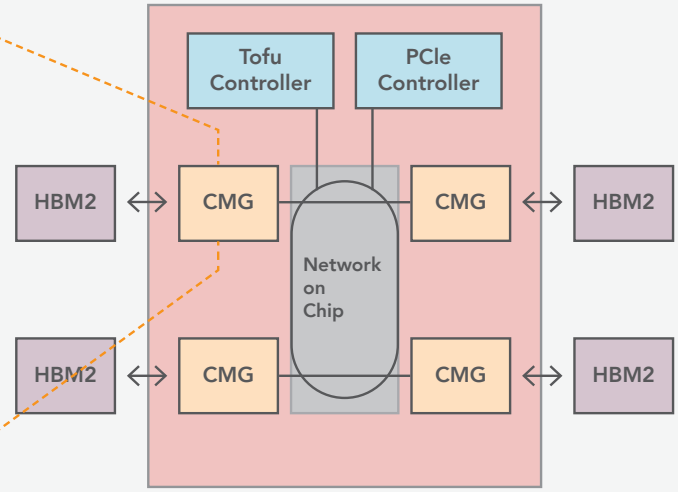
Four CMGs maintain cache coherence with on-chip directory

- Threads binding within a CMG allows linear speed up of core's performance

CMG Configuration



A64FX Chip Configuration



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